CLAIMS

We claim:

1. An image sensor, comprising:

a sensor array, including a two-dimensional array of pixel elements, that outputs digital signals as pixel data representing an image of a scene;

a data memory coupled to said sensor array and fabricated with said sensor array on a same integrated chip, said data memory for storing said digital pixel data; and

a logic circuit coupled to said data memory and fabricated with said data memory on said same integrated chip, said logic circuit providing a memory interface for exporting said pixel data.

2. The image sensor of claim 1, wherein said memory interface is a SRAM interface.

3. The image sensor of claim 1, wherein said memory interface is a DRAM interface.

4. The image sensor of claim 1, wherein said memory interface is a packet protocol synchronous DRAM interface.

5. An image sensor, comprising:

a pixel array, including a two-dimensional array of pixel elements, that outputs analog signals as pixel data representing an image of a scene;

an analog-to-digital converter coupled to said pixel array for converting said analog signals into digital pixel data;

a data memory coupled to said analog-to-digital converter and fabricated with said pixel array and said analog-to-digital converter on a same integrated chip, said data memory for storing said pixel data; and

a logic circuit coupled to said data memory and fabricated with said data memory on said same integrated chip, said logic circuit providing a memory interface for exporting said pixel data.

6. The image sensor of claim 5, wherein said memory interface is a SRAM interface.

7. The image sensor of claim 5, wherein said memory interface is a DRAM interface.

8. The image sensor of claim 5, wherein said memory interface is a packet protocol synchronous DRAM interface.

9. An image sensor, comprising:

a pixel array, including a two-dimensional array of pixel elements, that outputs analog signals as pixel data representing an image of a scene;

a data memory coupled to said pixel array and fabricated with said pixel array on a same integrated chip, said data memory for storing said pixel data; and

a logic circuit coupled to said data memory and fabricated with said data memory on said same

integrated chip, said logic circuit providing a memory interface for exporting said pixel data.

10. The image sensor of claim 9, wherein said memory interface is a SRAM interface.

11. The image sensor of claim 9, wherein said memory interface is a DRAM interface.

12. The image sensor of claim 9, wherein said memory interface is a packet protocol synchronous DRAM interface.

13. An image sensor, comprising:

a sensor array, including a two-dimensional array of pixel elements, that outputs digital signals as pixel data representing an image of a scene; and

a dual-port data memory, a first port of said dual-port data memory coupled to said sensor array for storing said pixel data, and a second port of said dual-port data memory providing a memory interface for exporting said pixel data, said dual-port data memory being fabricated with said sensor array on a same integrated chip.

14. An imaging system, comprising:

an image sensor, comprising:

a sensor array, including a two-dimensional array of pixel elements, that outputs digital signals as pixel data representing an image of a scene;

a data memory coupled to said sensor array and fabricated with said sensor array

on a same integrated chip, said data memory for storing said pixel data;

a logic circuit coupled to said data memory and fabricated with said data memory on said same integrated chip, said logic circuit providing a memory interface for exporting said pixel data; and

an image processing device including a memory interface port;

wherein said image sensor is coupled to said memory interface port of said image processing device and said image processing device accesses pixel data in said image sensor using a memory interface protocol.

15. The image sensor of claim 14, wherein said memory interface of said image sensor is a SRAM interface.

16. The image sensor of claim 14, wherein said memory interface of said image sensor is a DRAM interface.

17. The image sensor of claim 14, wherein said memory interface of said image sensor is a packet protocol synchronous DRAM interface.

18. A method in an image sensor, comprising:

capturing an image of a scene using a sensor array;

storing pixel data representative of said images in a data memory being fabricated on a same integrated circuit as said sensor array; and

outputting said pixel data to an image processing device using a memory interface protocol.

19. The image sensor of claim 18, wherein said memory interface protocol is a SRAM interface protocol.

20. The image sensor of claim 18, wherein said memory interface protocol is a DRAM interface protocol.

21. The image sensor of claim 18, wherein said memory interface protocol is a packet protocol synchronous DRAM interface protocol.